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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,545	11/26/2001	Peter Rabkin	00939A-085300US	8177

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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER
IM, JUNGHWA M

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/994,545	Applicant(s) RABKIN ET AL.	
	Examiner Junghwa M. Im	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *1-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 17-35 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "undoped polysilicon," used in each of the independent claims, is not clear. The specification describes a process in which polysilicon is deposited as undoped, but, as noted in the discussion of figure 5, the thermal processing required to produce a finished device results in diffusion of dopant into the "undoped" polysilicon from adjacent polysilicon which is deposited in doped form. (Figure 5 shows the dopant concentration of the "undoped poly" as greater than 102° impurity atoms cm-3, which is referred to as a relatively high dopant level at page 2, line 1, of the specification.) So "undoped polysilicon" could be understood to mean "undoped as deposited," although this requires reading something into the claim language that is not specifically stated. But the claims could also be attempting to describe an intermediate structure, i.e., a layered structure such as that of figure 2 of the specification which is not intended to describe a completed device. The problem with this interpretation is that the preamble of claim 17 states that the claim is drawn to a "non-volatile memory cell," which would have to be a completed device. because an intermediate structure would not be able to function as a "memory cell." Claim 26, similarly, is drawn to a "transistor," which is understood in the art to describe a device capable of functioning as a transistor, and not simply an intermediate structure. The claim

language "undoped" is thus not clear, because this term could mean "undoped as deposited," to correspond with the description of the specification, or the term could mean that claim language is describing an intermediate structure, rather than a finished device. If the second interpretation of "undoped" is the intended meaning, then the claim language of "memory cell" of claim 17, and "transistor" of claim 26, is not clear.

The following is a quotation of the first paragraph of 35 U. S. C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 17-35 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification does not appear to teach any way of making a finished device, such as a "memory cell" or a "transistor" which would have undoped polysilicon layers as recited in the claims. As noted in the specification, the thermal processing required to make a device would cause diffusion of dopant into undoped polysilicon, which would no longer be undoped. Even if the claimed structure is understood as being drawn to an intermediate or unfinished structure, deposition of a doped polysilicon layer on top of an undoped layer will involve a high temperature process, which will cause diffusion of dopant even during a single deposition step. Because the specification does not teach any way of avoiding dopant diffusion into an undoped layer during subsequent processing steps, one of ordinary skill would not be able, based on the specification, to fabricate "undoped" polysilicon layers adjacent to doped polysilicon layers as

required by each of the independent claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 26-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Yeh et al. (U.S. 5,840,607), hereafter Yeh.

Regarding claim 26, Fig. 4 of Yeh teaches a semiconductor transistor comprising:

an insulating layer 20 over a substrate;

an undoped polysilicon layer 22 over and in contact with the insulating layer; and

a doped polysilicon layer 24 over and in contact with the undoped polysilicon layer 22, the doped and undoped polysilicon layers forming a gate, (a floating gate, thus electrically accessible).

Regarding claim 27, Yeh discloses that the insulating layer is an oxide layer (col. 3, line 2).

Regarding claim 28, Yeh discloses that a thickness of each doped polysilicon is greater than a thickness of the undoped polysilicon layer by a factor in the range of two to four (col.3, lines 34-45).

Regarding claim 29, Yeh discloses the transistor further comprising:

insulating spacers (42) along sidewalls of the gate; and

source and drain regions in the substrate.

Regarding claim 30, Yeh discloses the doped polysilicon layer is in-situ doped with impurities (co. 3, lines 32-36).

In addition, note that "in-situ" is a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 31,Yeh discloses that the structure is a MOS transistor(col.1, line 24).

Regarding claim 32, it is inherent that the doped polysilicon layer of Yeh has a doping concentration since it's formed by using a doping process (col. 3, lines 32-32) and a thickness greater than a thickness of the undoped polysilicon layer (col.3, lines 22- 29). And the smaller grain size of undoped polysilicon layer reduces the impurity diffusion from the overlying doped polysilicon thus, preventing the gate oxide from degrading as taught in column 3, lines 23-45.

Regarding claim 33, Fig. 4 of Yeh discloses a semiconductor structure comprising:

an undoped polysilicon layer 22;

a doped polysilicon layer 24 in contact with the undoped polysilicon layer 22; and

an insulating layer 20 in contact with the undoped polysilicon layer 22, wherein the undoped polysilicon layer 22 is sandwiched between the doped polysilicon layer 24 and the insulating layer 20

Subject matters of claims 34 and 35 have been discussed previously.

Claim Rejections - 35 USC § 102/103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 26-27, 29-31, 33, and 35 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(x) as obvious over Chan et al.

Figure 1 of Chan et al. shows a transistor having a gate insulating layer 14 over substrate 10, with polysilicon gate 16, which is electrically accessible through the top layer of silicide 24. Column 1, lines 40-45, states that the gate electrode can be a multilayered structure having a doped polysilicon layer over an undoped layer. Such a gate electrode would correspond to the layer structure of claims 26 and 33, so the reference is anticipatory. Alternatively, it would have been obvious to form the polysilicon layer of Chan figure 1 as a doped polysilicon layer over an undoped layer, because this is what the reference suggests to do.

With respect to claim 27, Chan layer 14 is gate oxide. With respect to claim 29, Chan et al. shows spacers at 20 and source/drain regions 22. With respect to claim 30, the process limitation has not been shown to give rise to distinct structure from that taught by the reference. With respect to claims 31 and 35, the Chan device is either NMOS or PMOS, depending on the doping of source and drain.

Claims 26- 35 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Poon et al.

Figure 1 H of Poon et al. teaches a semiconductor structure comprising undoped polysilicon layer 15 (column 5, line 44), doped polysilicon layer 17, and insulating layer 14 in contact with the undoped polysilicon. The layers form part of a gate which is inherently, or

alternatively obviously, electrically accessible, because a voltage must be applied to the gate. Claim 33 thus appears to be anticipated. If claim 26 is understood to encompass an intermediate structure, rather than a finished device, then this claim is anticipated also. Structure recited in the dependent claims is clearly shown in the figure.

Claim Rejections - 35 USC § 103

Claims 28, 32, and 34 are rejected under 35 U.S.C. 103(x) as being unpatentable over Chan et al. in view of Krivokapic et al.

Column 2, lines 30-34, of Krivokapic et al. teaches that poly depletion effects in a polysilicon gate are undesirable because of altered workfunction. Absent any showing of criticality, it would have been obvious to optimize the polysilicon layer thicknesses and dopant concentrations of the Chan device, in order to minimize poly depletion effects, which are undesirable as taught by Krivokapic et al.

Claims 17- 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh et al. in view of Poon et al.

With respect to claim 17, Yeh et al. teaches in figure 4 each element of the claim except for a control gate having an undoped polysilicon layer beneath a doped polysilicon layer. Figure 1 H of Poon et al. teaches a gate electrode having an undoped polysilicon layer beneath a doped polysilicon layer. The paragraph spanning columns 5 and 6 of Poon et al. explains the reasons why the undoped polysilicon layer is advantageous. It would have been obvious to include an undoped polysilicon layer beneath the doped polysilicon layer of the Yeh control gate, for the reasons noted by Poon et al.

With respect to claims 18-19, 21-23, and 25; the recited structure is shown in Yeh figure 4. With respect to claims 20 and 24, layer 17 of Poon figure 1 H is shown as having a thickness of more than two times the thickness of layer 15.

Response to Arguments

Applicant's arguments with respect to claims 17-35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JMI
February 24, 2003

Sara Crane
Primary Examiner